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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/864,309	05/25/2001	Shigeyuki Uzawa	862.C2239	2803

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FITZPATRICK CELLA HARPER & SCINTO  
30 ROCKEFELLER PLAZA  
NEW YORK, NY 10112

EXAMINER

JARRETT, RYAN A

ART UNIT	PAPER NUMBER
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2125

DATE MAILED: 06/04/2003

5

Please find below and/or attached an Office communication concerning this application or proceeding.

124

# Office Action Summary

Application No.

09/864,309

Applicant(s)

UZAWA ET AL.

Examiner

Ryan A. Jarrett

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 25 May 2001.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-47 is/are pending in the application.
- 4a) Of the above claim(s) 23-35 and 45 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-22, 36-44, 46 and 47 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☒ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_ 6) ☐ Other: \_\_\_\_\_

**DETAILED ACTION**

***Election/Restrictions***

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:
  - I. Claims 1-11, 15, 21, 22, 36, 37, 39, 41, 42, 44, 46 drawn to a wafer exposure apparatus, classified in class 700, subclass 121.
  - II. Claims 23-27, drawn to a wafer processing method, classified in class 438, subclass 5.
  - III. Claims 28-35, drawn to a wafer transfer system, classified in class 414, subclass 935.
  - IV. Claim 45, drawn to a maintenance method, classified in class 702, subclass 184.
2. Claims 12-14, 16-20, 38, and 40 link inventions I and II. Claims 43 and 47 link inventions I and IV. The restriction requirement among the linked inventions is subject to the nonallowance of the linking claim(s), claims 12-14, 16-20, 38, 40, 43, and 47. Upon the allowance of the linking claim(s), the restriction requirement as to the linked inventions shall be withdrawn and any claim(s) depending from or otherwise including all the limitations of the allowable linking claim(s) will be entitled to examination in the instant application. Applicant(s) are advised that if any such claim(s) depending from or including all the limitations of the allowable linking claim(s) is/are presented in a continuation or divisional application, the claims of the continuation or divisional application may be subject to provisional statutory and/or nonstatutory double patenting rejections over the claims of the instant application. Where a restriction requirement is

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withdrawn, the provisions of 35 U.S.C. 121 are no longer applicable. *In re Ziegler*, 44 F.2d 1211, 1215, 170 USPQ 129, 131-32 (CCPA 1971). See also MPEP § 804.01.

3. During a telephone conversation with Steve Warner on 5/16/03 a provisional election was made with traverse to prosecute the invention of Group I, claims 1-11, 15, 21, 22, 36, 37, 39, 41, 42, 44, 46, and linking claims 12-14, 16-20, 38, 40, 43, and 47. Affirmation of this election must be made by applicant in replying to this Office action. Claims 23-35 and 45 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

4. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

### ***Claim Rejections - 35 USC § 112***

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 22 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 22, it is not clear what is meant by adjusting "an ambient atmosphere of a temperature controller."

***Claim Rejections - 35 USC § 102***

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1-21, and 36-41 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Ueda et al. U.S. Patent No. 6,319,322. Ueda et al. discloses an exposure apparatus for exposing a wafer to a pattern, comprising: a chamber that surrounds a predetermined space in the exposure apparatus; an air-conditioner for adjusting an internal atmosphere of the exposure apparatus; and a port section having a load-lock mechanism; wherein said port section comprises an exhaust mechanism for exhausting gas from said port section, and a supply mechanism for supplying gas into said-port section; wherein said port section comprises a door for shielding said port section from outside of the exposure apparatus, and a door for shielding said port section from said chamber; wherein said port section includes a plurality of port sections; wherein said port section includes a first port section for loading the wafer and a second port section for unloading the wafer; further comprising an interface for stocking a wafer between said port section and outside of the exposure apparatus; wherein said interface comprises a load-lock mechanism; wherein said interface is shared between a first port section for loading a wafer and a second port section for

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unloading the wafer; wherein said interface is interposed between said port section and a coating/developing system; wherein said port section comprises a temperature control mechanism for controlling a temperature of the wafer; wherein the temperature control mechanism comprises a heater for heating the wafer; wherein the heater heats the wafer; wherein the wafer to be heated is a wafer coated with a resist; wherein the heater heats an exposed wafer; wherein the temperature control mechanism comprises a cooler for cooling the wafer; wherein the cooler cools a heated wafer; wherein the temperature control mechanism controls the temperature of the wafer while an internal atmosphere of said port section is set close to an internal atmosphere of the exposure apparatus; wherein the temperature control mechanism controls the temperature of the wafer while gas in said port section is exhausted; wherein the wafer is heated while gas in said port section is exhausted; wherein the wafer is cooled while gas is supplied to said port section further comprising a temperature controller incorporated in said chamber to control a temperature of the wafer;

a device manufacturing system comprising: a coating/developing system having a resist coating unit for coating a wafer with a resist and a developing unit for developing the exposed wafer; an exposure apparatus for exposing the wafer to a pattern of a master; a port section which is interposed between said coating/developing system and said exposure apparatus and has a load-lock mechanism; and a temperature control mechanism incorporated in said port section to control a temperature of the wafer; wherein said port section comprises an exhaust mechanism for exhausting gas from said port section, and a supply mechanism for supplying gas

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into said port section; wherein said temperature control mechanism heats the wafer; wherein the wafer to be heated is a wafer coated with a resist; further comprising a controller for controlling to heat while an internal atmosphere of said port section is set close to an internal atmosphere of said exposure apparatus after the wafer is transferred to said port section;

a device manufacturing method comprising the steps of: installing manufacturing apparatuses for various processes of a device manufacturing system in a semiconductor manufacturing factory; and manufacturing a semiconductor device by using the manufacturing apparatuses in a plurality of processes, the device manufacturing system having a coating/developing system having a resist coating unit for coating a wafer with a resist and a developing unit for developing the exposed wafer, an exposure apparatus for exposing the wafer to a pattern of a master, a port section which is interposed between the coating/developing system and the exposure apparatus and has a load-lock mechanism, and a temperature control mechanism incorporated in the port section to control a temperature of the wafer (e.g. col. 1 line 32 – col. 2 line 43, col. 5 lines 1-53, col. 6 lines 33-67, col. 7 lines 20-40, col. 8 lines 15-67, col. 9 line 44 – col. 10 line 35).

### ***Claim Rejections - 35 USC § 103***

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

10. Claims 42-44, 46, and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ueda et al. as applied to claim 41 above, and further in view of La et al. U.S. Patent No. 5,761,064. Ueda et al. discloses many of the limitations of claims 42-44, 46, and 47 as illustrated above. Ueda et al. does not specifically disclose connecting the manufacturing apparatuses by a local area network; and communicating information about at least one of the manufacturing apparatuses between the local area network and an external network outside the semiconductor manufacturing factory; wherein a database provided by a vendor or user of the exposure apparatus is accessed via the external network to obtain maintenance information of the manufacturing apparatus by data communication, or production management is performed by data communication between the semiconductor manufacturing factory and another semiconductor manufacturing factory via the external network.; authorizing access from the semiconductor manufacturing factory to the maintenance database via the external network; and transmitting maintenance information accumulated in the maintenance database to the semiconductor manufacturing factory via the external network.

However, La et al. discloses a wafer defect management system for productivity and yield improvement that comprises connecting manufacturing apparatuses by a local area network; and communicating information about at least one of the manufacturing apparatuses between the local area network and an external network outside the semiconductor manufacturing factory; wherein a database provided by a vendor or user of the exposure apparatus is accessed via the external network to obtain maintenance



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information of the manufacturing apparatus by data communication, or production management is performed by data communication between the semiconductor manufacturing factory and another semiconductor manufacturing factory via the external network.; authorizing access from the semiconductor manufacturing factory to the maintenance database via the external network; and transmitting maintenance information accumulated in the maintenance database to the semiconductor manufacturing factory via the external network (col. 2 line 19 – col. 3 line 6). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Ueda et al. with La et al. since La et al. teaches that such a system would save time and cost expended by technicians gathering information for the engineers and increase product yields due to a faster correction of defect causes (col. 3 lines 7-20).

### ***Conclusion***

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Akimoto et al. U.S. Patent No. 5,980,591 discloses a system for processing a plurality of objects contained in a plurality of cassettes.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan A. Jarrett whose telephone number is (703) 308-4739. The examiner can normally be reached on 9:30-6:00 M-F.

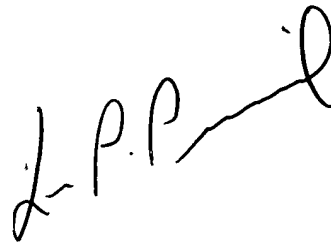
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached on (703) 308-0538. The fax phone numbers for

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the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

raj  
May 30, 2003

A handwritten signature in black ink, appearing to read 'L. P. Picard', written in a cursive style.

LEO PICARD  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2100